FAIRCHILD
SEMICONDUCTOR™

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FDS4501H

Complementary PowerTrench® Half-Bridge MOSFET

General Description

This complementary MOSFET half-bridge device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- DC/DC converter
- Power management
- Load switch
- Battery protection

Features

- **Q1**: **N-Channel**

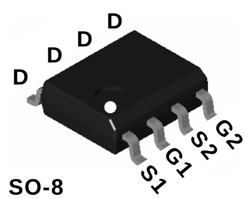
  9.3A, 30V $R_{DS(on)}$ = 18 mΩ @ V_{GS} = 10V

  $R_{DS(on)}$ = 23 mΩ @ V_{GS} = 4.5V

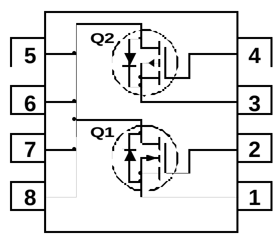
- **Q2**: **P-Channel**

  –5.6A, –20V $R_{DS(on)}$ = 46 mΩ @ V_{GS} = –4.5V

  $R_{DS(on)}$ = 63 mΩ @ V_{GS} = –2.5V



SO-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		30	–20	V
V_{GSS}	Gate-Source Voltage		±20	±8	V
I_D	Drain Current - Continuous	(Note 1a)	9.3	–5.6	A
	- Pulsed		20	–20	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5		W
		(Note 1b)	1.2		
		(Note 1c)	1		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Thermal Characteristics

Symbol	Parameter		Value	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4501H	FDS4501H	13"	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

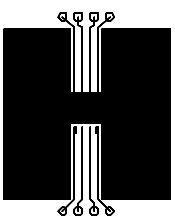
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA V_{GS} = 0 V, I_D = –250 µA	Q1 Q2	30 –20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = –250 µA, Referenced to 25°C	Q1 Q2		24 –13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = –16 V, V_{GS} = 0 V	Q1 Q2			1 –1	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V V_{GS} = ±8 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA V_{DS} = V_{GS}, I_D = –250 µA	Q1 Q2	1 –0.4	1.6 –0.7	3 –1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = –250 µA, Referenced to 25°C	Q1 Q2		–4 3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 9.3 A V_{GS} = 10 V, I_D = 9.3 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 7.6 A	Q1		14 21 17	18 29 23	mΩ
		V_{GS} = –4.5 V, I_D = –5.6 A V_{GS} = –4.5 V, I_D = –5.6 A, T_J = 125°C V_{GS} = –2.5 V, I_D = –5.0 A	Q2		36 49 47	46 80 63	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V V_{GS} = –4.5 V, V_{DS} = –5 V	Q1 Q2	20 –20			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 9.3 A V_{DS} = 5 V, I_D = –5.6 A	Q1 Q2		28 16		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		1958 1312		pF
C_{oss}	Output Capacitance		Q1 Q2		424 240		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		182 106		pF

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

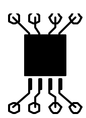
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω Q1 V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5V, R_{GEN} = 6 Ω	Q1 Q2		15 15	27 27	ns
t_r	Turn-On Rise Time		Q1 Q2		5 15	10 27	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		38 40	61 64	ns
t_f	Turn-Off Fall Time		Q1 Q2		10 25	20 40	ns
Q_g	Total Gate Charge	Q1 V_{DS} = 15 V, I_D = 9.3 A, V_{GS} = 4.5 V Q2 V_{DS} = 15 V, I_D = –2.4 A, V_{GS} = –4.5V	Q1 Q2		17 13	27 21	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		4 2.5		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		5 2.0		nC
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			2.1 –2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2) V_{GS} = 0 V, I_S = –2.1 A (Note 2)	Q1 Q2			1.2 –1.2	V

Notes:

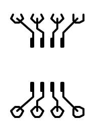
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in² pad of 2 oz copper



b) 105°C/W when mounted on a 0.04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics: Q2

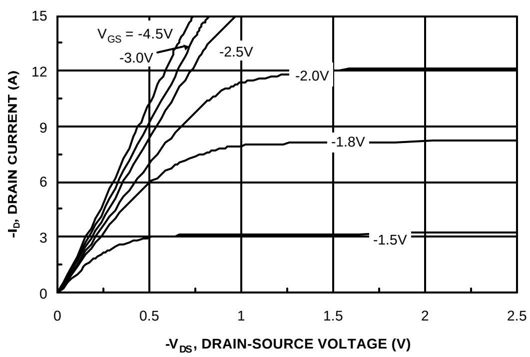


Figure 1. On-Region Characteristics.

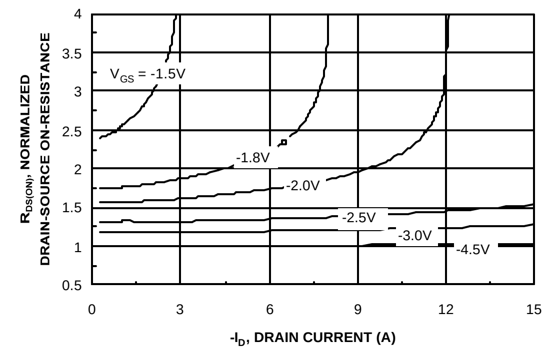


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

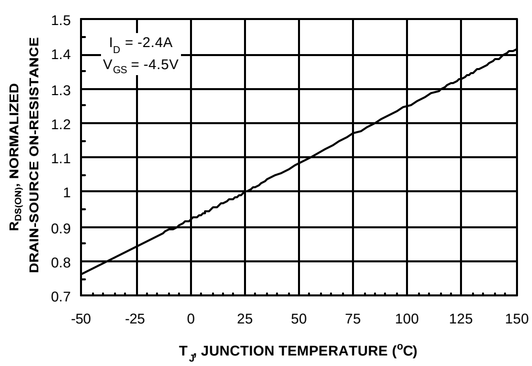


Figure 3. On-Resistance Variation with Temperature.

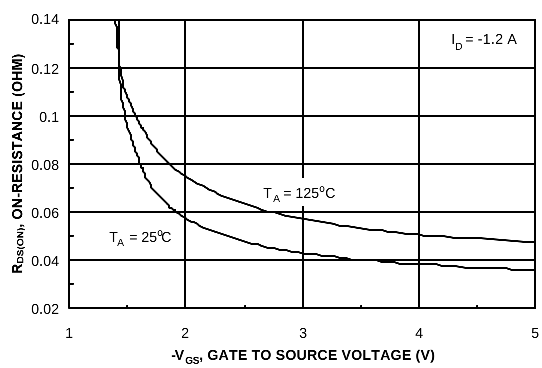


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

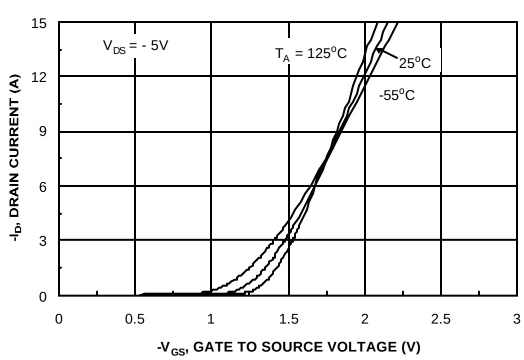


Figure 5. Transfer Characteristics.

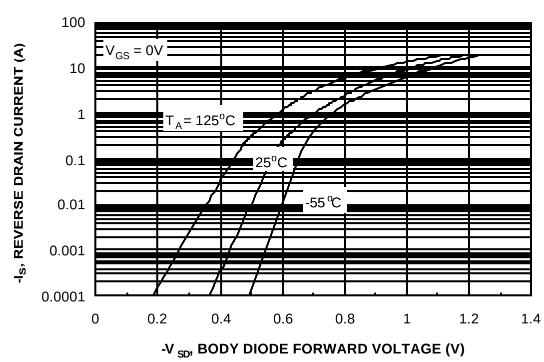


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

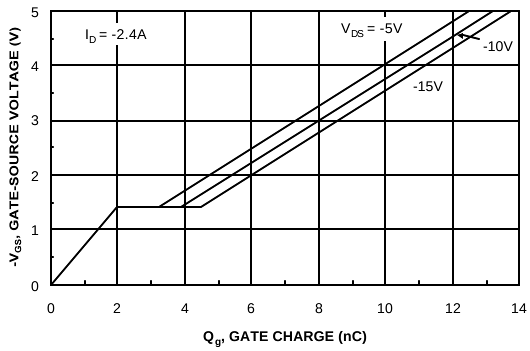


Figure 7. Gate Charge Characteristics.

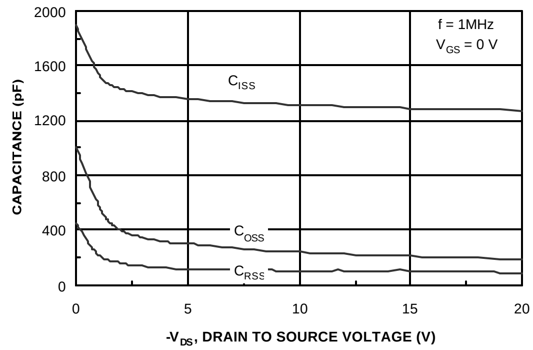


Figure 8. Capacitance Characteristics.

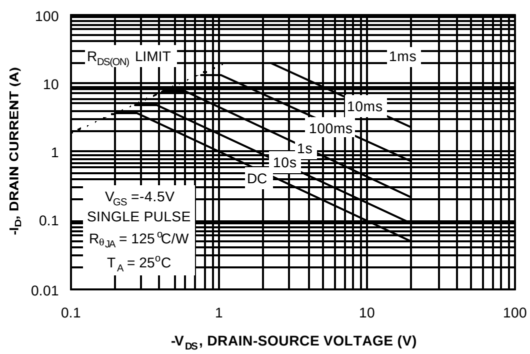


Figure 9. Maximum Safe Operating Area.

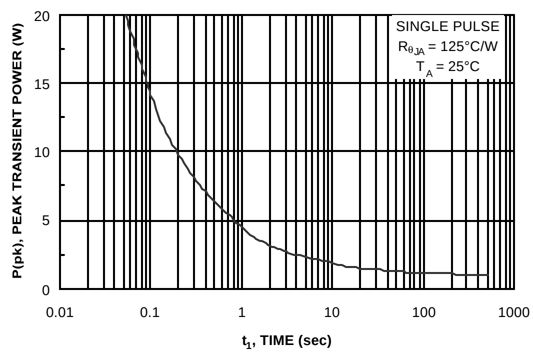


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q1

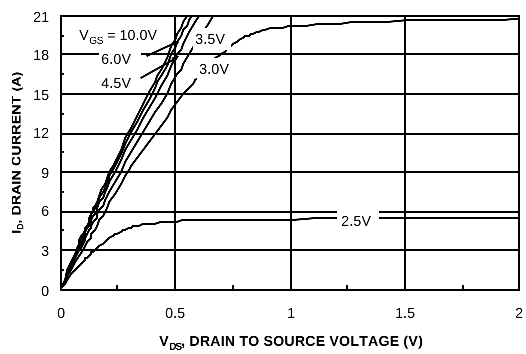


Figure 11. On-Region Characteristics.

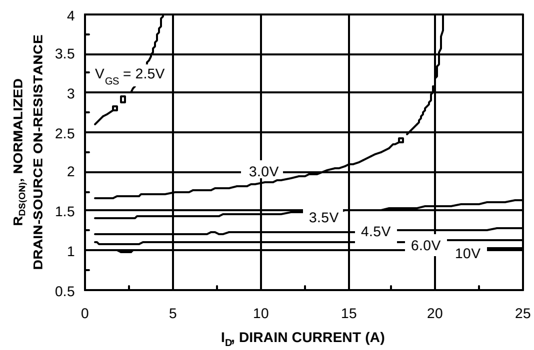


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

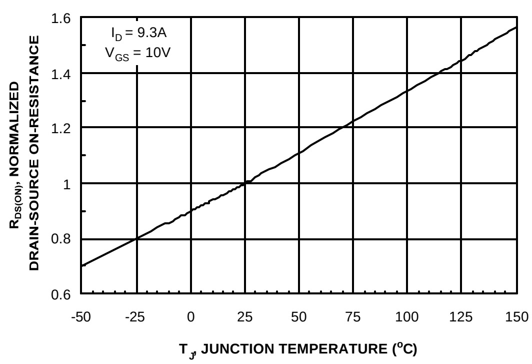


Figure 13. On-Resistance Variation with Temperature.

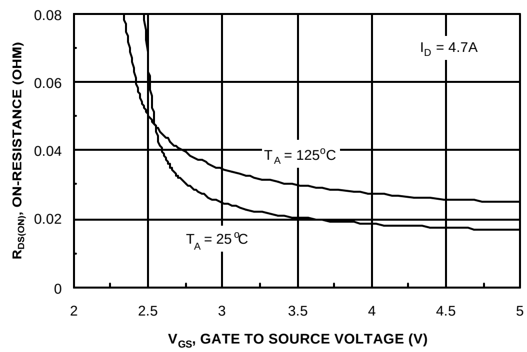


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

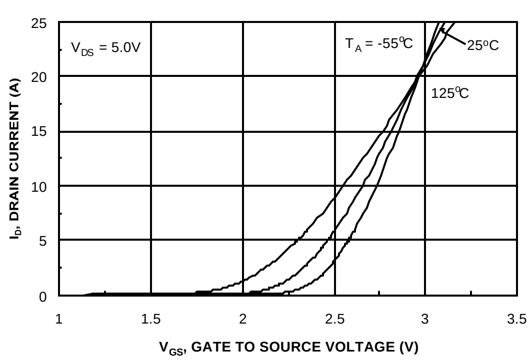


Figure 15. Transfer Characteristics.

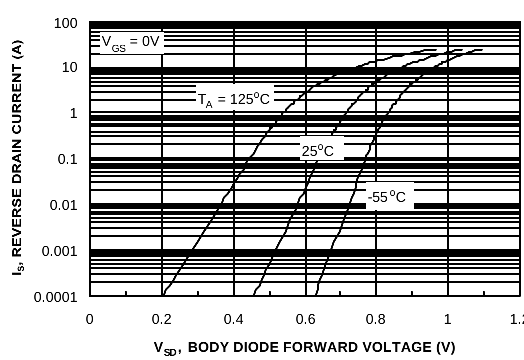


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics Q1

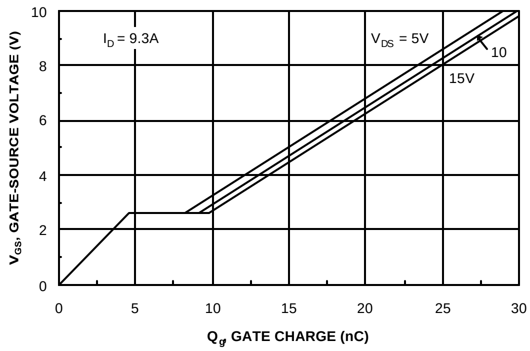


Figure 17. Gate Charge Characteristics.

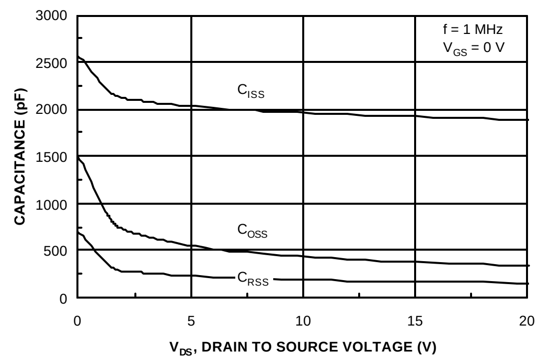


Figure 18. Capacitance Characteristics.

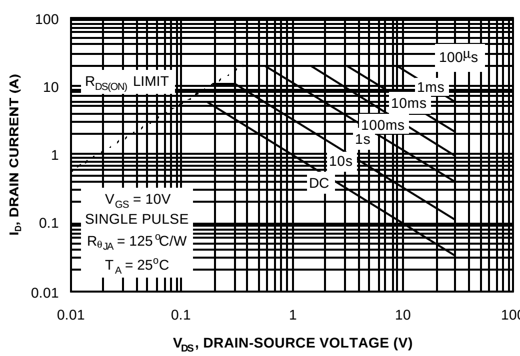


Figure 19. Maximum Safe Operating Area.

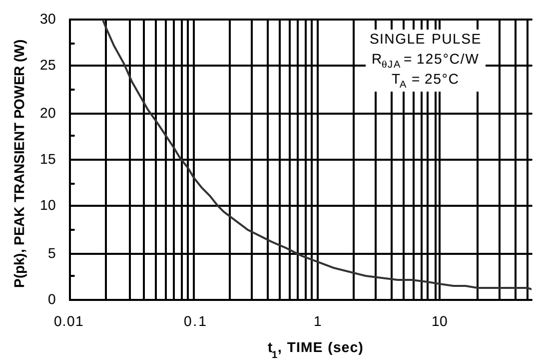


Figure 20. Single Pulse Maximum Power Dissipation.

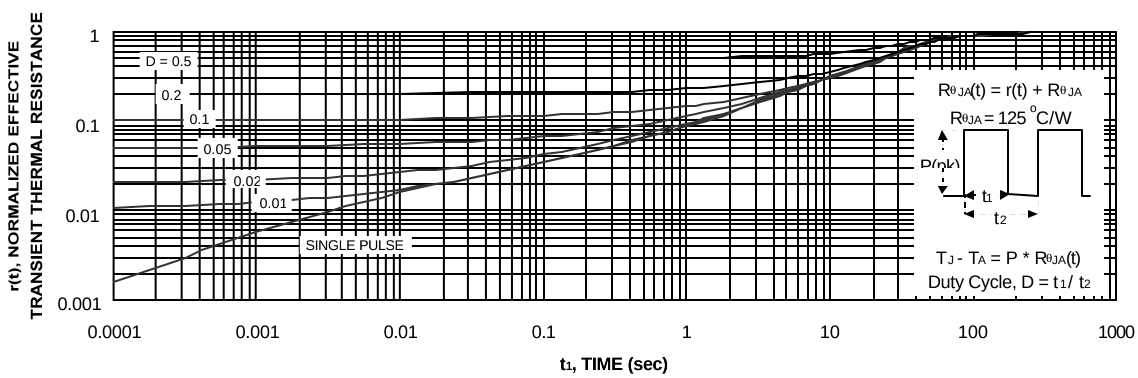


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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